John L. Cooper (State Bar No. 050324)
jcooper@fbm.com
Stephanie Powers Skaff (State Bar No. 183119)
sskaff@fbm.com
Eugene Y. Mar (State Bar No. 227071)
emar@fbm.com
Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
Telephone: (415) 954-4400
Facsimile: (415) 954-4480

Attorneys for Defendants
TECHNOLOGY PROPERTIES LTD. and
ALLIACENSE LTD.

Charles T. Hoge, Esq. (State Bar No. 110696)
choge@knlh.com
Kirby Noonan Lance & Hoge
35 Tenth Avenue
San Diego, CA 92101
Telephone: (619) 231-8666
Facsimile: (619) 231-9593

Attorneys for Defendant
PATRIOT SCIENTIFIC CORPORATION

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED,

Defendants.

Case No. 5:08-cv-00877 JF/HRL

DEFENDANTS' CLAIM CONSTRUCTION REPLY BRIEF

[RELATED CASES]

Date: TBD
Time: TBD
Dept: Courtroom 3, 5th Floor
Judge: Hon. Jeremy Fogel

HTC CORPORATION and HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00882 JF/HRL
BARCO, N.V., Plaintiff, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-05398 JF/HRL

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

TABLE OF CONTENTS

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

TABLE OF AUTHORITIES

Page

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

I. INTRODUCTION

Plaintiffs are proposing that the majority of claim terms in dispute do not mean what they say, but rather have been narrowed due to a number of disclaimers. In each case, Plaintiffs' showing falls far short of the "clear and unequivocal" standard required to establish a disclaimer. Their consistent overreaching actually confirms the breadth of the patents-in-suit. Plaintiffs also try to reargue the issues that were before Judge Ward based on events in later reexaminations; however, they provide only partial evidence, hold back key inventor amendments, and misinterpret the evidence they do provide. Their strained readings do not justify narrow constructions. When they are not pursuing disclaimer theories, Plaintiffs try to limit the claims to some embodiments, while reading out others. TPL's constructions, on the other hand, are supported by the intrinsic evidence and give the claims their full and proper scope.

II. CONSTRUCTION OF DISPUTED CLAIM TERMS

A. "Ring Oscillator" and Related Terms

1. "Ring Oscillator" (Joint Claim Construction Statement ("JCCS") Row 22)

Defendants' construction of ring oscillator is correct, because the patent owner did not disclaim anything in distinguishing the Talbot reference (U.S. Patent No. 4,689,581 ("Talbot")) in reexamination of the '148 patent. Talbot disclosed a voltage-controlled oscillator, but not the claimed ring oscillator. Plaintiffs fixate on three sentences of an examiner's interview summary that suggested a ring oscillator was "non-controllable," without disclosing that the patent owners promptly filed a written response to the summary pointing out that while Talbot disclosed two oscillator implementations, "neither [wa]s a ring oscillator." 2/21/2008 '148 Reexam Hist., Chen Dec., Ex. H, 11. "As the sole inventor of the cited reference, Talbot presumably possesse[d] at least ordinary skill in the art, yet Talbot did not characterize either of the disclosed oscillators as ring oscillators." *Id.* The examiner accepted TPL's argument that the "specific features" of Talbot's oscillator circuits, while including a voltage-controlled oscillator ("VCO"), "[were] unclear if the components actually ma[d]e a ring oscillator." '148 Reexam Hist., Gupta Dec., Ex. 1, TPL0019232. The subsequent allowance over Talbot was therefore not about the

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

controllability (or lack thereof) of a ring oscillator, but instead reflected the examiner's conclusion that Talbot did not disclose a ring oscillator. Disclaimer does not apply. *See Omega Eng'g, Inc v. Raytek Corp.*, 334 F.3d 1314, 1324-25 (Fed. Cir. 2003) ("We have … declined to apply the doctrine of prosecution disclaimer where the alleged disavowal of claim scope is ambiguous." (collecting cases)). [1]

Furthermore, Plaintiffs wrongly argue that the ring oscillator must be "non-controllable" (a phrase used by the examiner, not TPL, in the interview summary) or "free running" (an undefined term from the inventors' depositions) in order to improve CPU performance. The phrases "non-controllable" and "free running" were not used by the inventors in the specification or prosecution history, nor has TPL suggested they account for a microprocessor's increased performance. The improvement is enabled by having an on-chip oscillator as opposed to an off-chip oscillator, not an oscillator that is "non-controllable" versus "controllable." Even so, the on-chip oscillator capability varies together with the CPU's capability so that the CPU can operate at a maximum possible frequency, not that it always does so. *See e.g.*, '336, claim 1, 11, Mar Dec. Ex. H. It is undisputed that a ring oscillator can be controlled by its voltage. Opposition Br. ("Opp.") 15.

Finally, the testimony of inventors Charles Moore (given as TPL's 30(b)(6) witness in the Texas litigation) and Russell Fish (deposition in the Texas litigation) created no "admission" or disclaimer, as is evident by Judge Ward's construction of the term "ring oscillator" in that case. Plaintiffs' arguments do not withstand scrutiny, and Defendants' construction should be adopted.

[1] *See also, Univ. of Pittsburgh v. Hedrick*, 573 F.3d 1290, 1297 (Fed. Cir. 2009) ("A wide chasm exists between the weak inference from the [interview] summary ... and a clear and unmistakable disavowal as required to limit a claim term."); *Purdue Pharma L.P. v. Endo Pharm. Inc.*, 438 F.3d 1123, 1136 (Fed. Cir. 2006) (patentee did not limit claims where it discussed properties of the invention during prosecution, but did not identify the properties "as a necessary feature of the claimed" invention, because the claims did not contain the limitation) (emphasis added); *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1124 (Fed. Cir. 2004) ("examiner and applicant talking past one another"; "[T]he record finally reflects the examiner's acquiescence to the claim language chosen by the applicant. This is not clear evidence of the patentee's disavowal of claim scope."); *see also*, n.2 (examiner's statement cannot amend claim).

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

2. "Does not directly rely on a command input … to generate a clock signal" (JCCS Rows 19, 23, 28)

Plaintiffs' attempt to improperly narrow Judge Ward's prior construction of "an entire ring oscillator variable speed system clock in a single integrated circuit" to exclude "directly" and "command input" hinges entirely on the notion that the claimed oscillator is "non-controllable."

TPL did not disclaim any ring oscillator controlled by a reference signal or a control signal, as Plaintiffs contend. Opp. 6-8. TPL disclaimed only off-chip oscillators clocking the CPU. Further, Dr. Oklobdzija is correct that a VCO is now almost universally implemented as a ring oscillator, but Talbot, a 30-year old design, provided two different implementations of the VCO 12 in Figs. 3-4, neither of which is a ring oscillator. Talbot, Figs. 3 -4, Chen Dec., Ex. B.

3. Judge Ward Agrees That The Patent Does Not Require The CPU To Execute At The "Maximum Frequency Possible." (JCCS Row 20)

Plaintiffs distort the prosecution history to suggest that the applicants distinguished Sheets by relying upon the "aspect" of the invention that the "CPU executes at the fastest speed possible." Opp. 9-10. This is incorrect. The applicants distinguished Sheets because it did not have an on-chip oscillator. '336 Pros. Hist., Mar Dec., Ex. C, TPL0001904 (emphasis in original) ("the present invention is directed to a system and method for clocking a central processing unit disposed *within the same integrated circuit*…"). The patent owner then amended claims to "explicitly recite that the ring oscillator and microprocessor are provided within the same integrated circuit." *Id.* Thus, the distinguishing factor is the presence of an on-chip oscillator, not the frequency of the CPU.

Plaintiffs are once again seeking to narrow a construction from Judge Ward, even though the Texas court already considered – and rejected – the exact same argument. *See* Ward 13-15 (Mar Dec., Ex. A) (rejecting argument that the same specification cites ('336 patent 17:1-2, Mar Dec., Ex. B) and prosecution history (Mar Dec., Ex. C, TPL0001905-06) that Plaintiffs rely on here require the CPU's processing frequency to be limited to the "fastest safe operating speed"). The patentees mentioned a "fastest safe operating speed" only in responding to an office action, noting that "the present invention [] provide[s] a variable speed clock for the microprocessor …

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

[which] allows the microprocessor to operate at its fastest safe operating speed." '336 Pros. Hist., Mar Dec., Ex. D, TPL0001919-20. This variable speed clock means that the microprocessor is merely capable of operating at its fastest operating speed, not that it must do so. Plaintiffs' proposed limitation should be rejected.

B. "Push Down Stack" and Related Terms

TPL's constructions for push down stack and the related terms covering the connection of the first push down stack to an Arithmetic Logic Unit (ALU) remain correct, because the inventors (1) never limited the invention to "hardware stacks" and (2) never defined or disclaimed the function of the connection between the ALU and first down stack as "direct coupling such that source and destination addresses are not used."

1. Plaintiffs Have All But Conceded Their Hardware Stack Theory. (JCCS Row 2)

The parties agree that the term "push down stack" refers to a "last-in first out" (LIFO) data structure. TPL contends this term includes the spectrum of possible stack implementations, including the disclosed RAM embodiments, and not just "hardware stacks" "organized from top to bottom" using physical "propagation" as Plaintiffs and their expert, Dr. Wolfe, argue.

a. Plaintiffs' Silence On The Stack Pointer Embodiments Undermines Their "Hardware Stack" Theory.

In its opening, TPL highlighted the patents' variety of stack structures including ones in which data storage elements are not "organized from top to bottom." Figures 2, 13 and 21 all show the use of stack pointers to operate stacks, including ones organized in RAM. Opening Brief ("Op. Br.") 4:16-6:24. Plaintiffs' telling silence on the fact that their construction reads out such preferred embodiments as stack pointer implementations confirms that TPL's construction is correct.

b. The Inventors Never Agreed To The Examiner's Passing Remark Regarding "Propagation," So It Does Not Support A Disclaimer.

Plaintiffs' only shred of support for a hardware stack structure is the examiner's statement in prosecution that data in stacks "propagates," but an examiner's remark in passing does not

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

constitute a disclaimer. *3M Innovative Props. Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1373 (Fed. Cir. 2003) ("Prosecution history ... cannot be used to limit the scope of a claim unless the ***applicant*** took a position before the PTO.") (emph. in original; citation omitted). Moreover, TPL never "agreed" with the examiner's use of the word "propagate."

The examiner rejected a claim for indefiniteness for failure to disclose the structure. He stated "the components (means for storing a top item, means for storing a next item and at least one stack register) of the first push down stack as recited do not appear to render the push down stack to operate as a stack." '749 Pros. Hist., Chen Dec. Ex. R, 3. He also noted his belief that "inputted items propagate," that the claimed stack did not do that, and that "the claim fails to recite how the components of the stack are interconnected so as to form a stack having stages between the input and output of the stack." *Id.*

The inventors responded with the very limited agreement that, "as the Examiner correctly notes, [the means for storing the top and next item, and at least one stack register] do not render the first push down stack to operate as a stack. These items are in addition to the conventional construction of the first push down stack which allow it to operate as a stack." '749 Pros. Hist., Chen Dec., Ex. S, 9. They overcame the indefiniteness rejection by introducing the modifier "further" before these elements in the claim to emphasize that "the recited language is in addition to conventional organization of the stacks which allow them to operate as stacks." *Id.*; Gupta Dec. Ex. 2, TPL0001111, allowing claim 6. As the patentee claimed no additional structure and was notably silent on the examiner's use of the word "propagate," there was no disclaimer.[2] Ironically, in attempting to limit the stack structure to physical propagation, Plaintiffs pass over the examiner's express observations that the applicant ***had not*** disclosed the stack structure and ***did not*** disclose propagation, and the inventors' subsequent affirmation that the stack structure was ***not disclosed***.

[2] *See Salazar v. Procter & Gamble Co.*, 414 F.3d 1342, 1345, 1347 (Fed. Cir. 2005), which stressed that "[a]n examiner's statement cannot amend a claim," and that "an applicant's silence regarding such statements does not preclude the applicant from taking a position contrary to the examiner's statements when the claim terms are construed during litigation."

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

2. The Connection Between The ALU And First Push Down Stack Is Not Limited To "Direct Coupling … Such That Source And Destination Addresses Are Not Used." (JCCS Rows 1, 3, 9(a), 9(b) 15, and 16)

Rather than construe the connection of the ALU and first push down stack according to the plain meaning of the term "connected to," Plaintiffs propose importing an unclaimed "direct coupling" limitation and prohibiting any use of source and destination addresses whatsoever.[3] The meaning of "connected to" is readily ascertainable as "connected to convey signals to," and should be construed in its full breadth. *See* section C. As explained below, neither the specification nor the prosecution manifests an "intentional disclaimer or disavowal, of claim scope by the inventor" and Plaintiffs' functional limitation is improper. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) (*en banc*). The disclaimer cases cited by Plaintiffs, including *Microsoft Corp. v. Multi-Tech Systems, Inc.*, 357 F. 3d 1340 (Fed. Cir. 2004), confirm the high quantum of proof necessary to show a disavowal, and that standard is not met here. *See also, Omega Eng'g Inc.*, 334 F.3d at 1324-25.

a. Requiring "Direct coupling" Reads Out A Preferred Embodiment.

Plaintiffs' "direct coupling" limitation implies that the top and next registers of the push down stack are "dedicated" so that no source and destination addresses are required. However, the use of dedicated registers is not an "essential aspect of the invention" and cannot support Plaintiffs' proposed "implied addressing" requirement. Opp. 19-20.[4] Plaintiffs import this limitation from one description of one embodiment, and in doing so read out at least one other disclosed embodiment that does not have dedicated top and next registers. Figure 13 portrays stack 74 connected to the ALU, where stack elements are addressed by a stack pointer. Because

[3] Plaintiffs are confused as to whether they are proposing that "'addresses' ***need not be*** explicitly specified in the instruction," as they have argued (Opp. 19:23-20:5 (emph. added)), or whether they categorically "***are not***" used, as they have proposed.

[4] Descriptions in the specification other than the ones Plaintiffs cite clearly utilize the broader claim term "connected to" to describe the ALU/first push down stack connection. *See e.g.*, '749 patent, 3:3-15; 6:28-33, Mar Dec., Ex. M. A broad claim term is not limited to one description of one embodiment. *See Phillips*, 415 F.3d at 1323 (claims should not be confined to embodiments); *Acumed LLC v. Stryker Corp.*, 483 F.3d 800, 807-809 (Fed. Cir. 2007) (rejecting an attempt to limit the term "transverse holes" to perpendicular holes based on a feature of the preferred embodiment, where the claim term "transverse" was broader than the term "perpendicular" used in the specification); *Varco, L.P. v. Pason Sys. USA Corp.*, 436 F.3d 1368, 1375 (Fed. Cir. 2006).

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

which element is top and which is next depends on the stack pointer, they are not "directly coupled." As Plaintiffs' construction would read out this non-direct coupling, non-dedicated, embodiment, it is incorrect.[5] Because the claims are not limited to direct coupling, this proposed limitation cannot be a springboard for a sweeping disclaimer of any and all source and destination addressing, as Plaintiffs argue.

b. The Core Inventions Of The '749 And '890 Patents Were Unrelated To Implied Addressing.

In contrast to cases like *Microsoft*, where the invention was "clearly" limited,[6] the core inventions of the '749 and '890 patents were unrelated to the proposed "implied addressing" limitation. Indeed, direct coupling of input registers for implied addressing purposes to reduce instruction size was already of record in the '749 patent file history. *See, e.g.*, Gupta Dec., Ex. 3 ('749 IDS discussing Moore, US 5,070,451).

The examiner also confirmed that implied addressing was not the invention when he interposed an early restriction requirement that delineated ten different inventions, all of which became separate applications. '749 Pros. Hist., Gupta Dec., Ex. 4. The application that matured into the '749 patent was directed to "a processor system having means for fetching multiple instructions in parallel during a single machin[e] cycle…." *Id.*, TPL0001069. Thus, multiple instruction fetch was the invention of the '749 patent, not implied addressing.

The '890 patent invention, as identified by the examiner, was a microprocessor architecture that included, among other things, a dual stack architecture wherein each stack has both a stack pointer and further has a separate element to which it is connected comprising its top

[5] *See Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1377 (Fed. Cir. 2005) (a construction that reads out a preferred embodiment, is "rarely if ever [] correct"); *Dow Chem. Co. v. Sumitomo Chem. Co.*, 257 F.3d 1364, 1378 (Fed. Cir. 2001) (expressly rejecting argument that claims need not read on some embodiments; "bolstered by the fact that the alternative would exclude many of the preferred embodiments"); *Interactive Gift Express, Inc. v. CompuServe, Inc.*, 231 F.3d 859 (Fed. Cir. 2000) (disfavoring constructions that read out preferred embodiments).

[6] The specification in *Microsoft* "ma[de] clear that the invention does not include a particular feature" of working on non-telephone lines because it "repeatedly and consistently describe[d] the local and remote systems of the claimed inventions as communicating directly over a telephone line" and "characterize[d] the entire 'personal communications system' as enabling communications between a local site and a remote site over a telephone line." 357 F.3d at 1347-48.

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

of stack. *Id.*, TPL0001070. This invention also did not mandate direct coupling and implied addressing such that source and destination addresses are not used.

c. Far From Requiring Implied Addressing, The Specification Affirmatively Discloses The Use Of Addressable Stacks.

The presence of addressable stacks further confirms that the Plaintiffs' proposed construction is wrong, as it would read out a preferred embodiment. Plaintiffs concede that Return Stack 134 is a register file that has addresses and is in fact addressed by instructions. '749 patent, Fig. 2, Mar Dec., Ex. M; Opp. at 8, 21; *see* '749 patent, 31:59-32:16 ("Read the XXXXth location relative to the top of the Return Stack."). The distinct function of the return stack is irrelevant, because it is clear that any stack can be addressable. In fact, the parameter stack 74 of Fig. 13 is also comprised of addressable registers and may be addressed in the same way as Return Stack registers.

Plaintiffs rely on prosecution history that simply says the ALU receives and supplies operands, but is silent as to implied addressing.[7] On the other hand, the MMP inventors made clear during prosecution that any stack can "posses[s] an organization which emulates registers," and that a register file is addressable. Op. Br. 8; Mar. Dec., Ex. N, TPL0001097. The prosecution history of these patents, accordingly, does not come close to establishing a disclaimer, as was found in cases like *Microsoft*, where there were "clear" limiting statements in prosecution. 357 F.3d at 1347.

d. The Measured Language Of The Patents And Prosecution History Cannot Support A Disavowal.

Claim scope was not disclaimed here because, in contrast to cases like *Microsoft*, the specification's language never gave up the use of source and destination addresses.

The bulleted passages relied on by Plaintiffs, when read carefully, demonstrate that the inventors actually envisioned the ***continued*** use of source and destination addresses (emphases added):

[7] "The stack 74 allows arithmetic operations to be carried out on operands supplied from it to the ALU and receives ALU results as a result of the recited connections." Opp. 21:18-20.

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

- "The push down stack ***allows*** the use of implied addresses" but it does not exclusively ***require*** or ***mandate*** the use of implied addresses. '749 patent, 7:19-21, Mar Dec., Ex. M.
- "A stack has advantage of faster operation compared to on-chip registers by avoiding the ***necessity*** to select source and destination registers" but it does not ***preclude*** the selection of source and destination registers. *Id.*, 15:28-32.
- "***Most*** of the work in the microprocessor 50 is done by the 8-bit instructions" but the specification does not say ***all*** work is done by 8-bit instructions. *Id.*, 25:65-66.
- "Eight bit instructions are possible with the microprocessor because of the ***extensive*** use of implied stack addressing" but ***extensive*** use does not equate to ***exclusive*** or even ***predominant*** use of implied stack addressing. *Id.*, 25:66-68.

The patents accordingly do not amount to a clear and unequivocal disavowal of source and destination addressing.[8]

e. Means-Plus-Function Elements (JCCS Row 8).

TPL properly construes the corresponding means plus function claims' function as "ordinary meaning," rejecting the additional functional limitations proposed by Plaintiffs. *Wenger Mfg., Inc. v. Coating Mach. Sys., Inc.*, 239 F.3d 1225, 1232 (Fed. Cir. 2001) ("Under § 112, 6, a court may not import functional limitations that are not recited in the claim, or structural limitations from the written description that are unnecessary to perform the claimed function"). Plaintiffs' criticism that TPL's identification of the corresponding structure as a "register or its equivalents" would result in any register "regardless of its structure or purpose" infringing is legally incorrect; TPL will still have to demonstrate that the register or its equivalent

[8] Similar measured statements did not support a disavowal in *Silicon Graphics, Inc. v. ATI Tech., Inc.*, 607 F.3d 784, 790 (Fed. Cir. 2010). The court held that "a rasterization process" was not required to "operate on a floating point format 'as a whole'" because (1) "[n]owhere [did] the specification teach that ***all*** rasterization processes must operate on a floating point format," (2) rasterization instead "***predominately operate***[d]" on a floating point format," and (3) "***certain*** rasterization processes [were] performed according to a floating point format." *Id.* at 790-91 (bold emph. added). This measured terminology is similar to the MMP patents "allowing" implied addressing, and avoiding the "necessity" to select source and destination addresses. As in *Silicon Graphics*, there was no disavowal. By contrast, the *Silicon Graphics* court properly construed a different term as being "on an entirely floating basis," where the specification clearly stated that particular process was "now handled ***entirely*** on," and "performed exclusively in," a floating point basis." 607 F.3d at 791 (bold emph. added). The non-absolute terminology used here does not rise to such a level.

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

performs the claimed function—roughly, storing a top/next item connected to a first/second input of said ALU to provide the item to the input. *See Vulcan Eng'g Co. v. Fata Aluminum, Inc.*, 278 F.3d 1366, 1373-74 (Fed. Cir. 2002) ("Infringement is found literally if the claimed function is performed by either the structure described in the patent or an equivalent of that structure.").

C. "Connected to" (JCCS Row 10)

TPL's proposed construction, "connected to convey signals to," properly accords with the intrinsic evidence and the "ordinary and customary meaning" of "connected to." *Phillips*, 415 F.3d at 1312. The specification, claims and figures of the MMP are rife with "connections" defining the signal pathways for the various devices on an integrated circuit practicing the invention. *See* e.g., '749 patent, claim 1, 6:24-56; '890 patent, claim 1, Mar Dec., Exs. M, K.

Plaintiffs' proposal to construe "connected to" "depend[ing] upon how the connected components are supposed to interact," should be rejected because it would violate the maxim that a "claim term should be construed consistently with its appearance in other places in the same claim or in other claims of the same patent." *Rexnord Corp. v. Laitram Corp.*, 274 F.3d 1336, 1342 (Fed. Cir. 2001). "Connected to" in these patents is a classic example of "[a] word or phrase used consistently throughout a claim" – it defines the integrated circuit layout – and accordingly "should be interpreted consistently" throughout the claims. *Epcon Gas Sys., Inc. v. Bauer Compressors, Inc.*, 279 F.3d 1022, 1030-31 (Fed. Cir. 2002).[9]

Plaintiffs' globally context-dependent approach also overlooks that where the inventors envisioned special functions for circuit connections, they expressly claimed them. *See id., e.g.* '749 patent, claim 1, Mar Dec., Ex. M ("***connected to*** a first input of said arithmetic logic unit ***to provide the top item to the first input***"). *See also, Kara Tech., Inc. v. Stamps.com, Inc.*, 582 F.3d 1341, 1347-48 (Fed. Cir. 2009) (refusing to restrict claims that did not recite the use of a "key", because when the inventor wished to so restrict the claims he did so explicitly); *cf. Phillips*, 415 F.3d at 1324-25 (opting against importing function not expressly claimed, where function

[9] *Microprocessor Enhancement Corp. v. Texas Instruments, Inc.*, 520 F.3d 1367, 1376 (Fed. Cir. 2008) is distinguishable because there the term had a "nonsensical reading under a uniform construction." There is nothing nonsensical about "connected to" in the MMP. Similarly, "connected to" is nothing like "substantially," a word which is inherently approximate, and accordingly must be understood by its context.

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

expressly claimed elsewhere).

The prosecution history distinguishing Kato, which Plaintiffs mischaracterize, actually supports TPL's position. The Examiner based his rejection on his contention that everything on the same chip was "connected." '336 Reexam Hist., Gupta Dec. Ex. 5, TPL0548530. TPL's proposed construction ***avoids*** this overly broad construction by requiring a connection to ***convey signals***. TPL's construction would permit one of skill in the art to concretely identify infringing structure without any confusion as to whether every device on the chip is connected. It is correct.

D. "Main CPU" And "Separate DMA CPU"

1. "Main CPU" (JCCS Row 11)

Rather than adopt Judge Ward's construction of CPU, Plaintiffs seek to exclude the main CPU from performing any DMA-related operations. Yet the specification manifests no disclaimer of particular functions from the CPU, and it is undisputed that a CPU can "perform direct memory access related operations."[10] The mere presence of a DMA CPU on the integrated circuit should not ***prevent*** the CPU from performing direct memory functions. *See Schwing GmbH v. Putzmeister AG*, 305 F.3d 1318, 1323-25 (Fed. Cir. 2002) ("the applicant's remarks [were not] sufficient to overcome the general rule that functional limitations should not be read into purely structural claims."). TPL's construction tracks Judge Ward's, and remains correct.

2. "Separate DMA CPU" (JCCS Row 14)

TPL's construction properly captures the essential function of a DMA CPU, "reading and writing to memory." Though Plaintiffs would like to limit the DMA CPU to structure 72, which "has the ability to fetch and execute instructions," Figure 9 clearly discloses "a ***more traditional*** DMA controller" (314) that is nevertheless labeled a "DMA CPU." '890 patent, 8:66-9:5, Mar Dec., Ex. K. Plaintiffs' argument that Figure 9 is somehow not relevant because the passage cited does not reference Figure 9, is unavailing. DMA CPU 314, the "more traditional DMA controller," only appears in Figure 9. Because Plaintiffs' construction would read out this preferred embodiment, it "would rarely if ever be correct." *See*, cases at n.5.

[10] In arguing that "the purpose of the DMA CPU is to relieve the main CPU of the burden of performing direct memory access functions," Plaintiffs impliedly concede that the main CPU is capable of performing DMA related functions.

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

Plaintiffs' construction of DMA CPU is also improper because it attempts to categorically prohibit any use of the main CPU by the DMA CPU. The passage relied on by Plaintiffs states only that, under some embodiments of the invention, "***DMA*** does not ***require*** use of the main CPU ***during DMA requests and responses***…" '890 patent, 2:2-4, Mar Dec. Ex. K (emph. added). This clearly leaves open the possibility of using the CPU outside of DMA requests and responses. Further, not ***requiring*** the use of the main CPU does not ***prohibit*** its use. TPL's construction properly captures the breadth of this term.

E. "Originates From A Source Other Than" (JCCS Rows 25, 26 and 27)

TPL's construction "generated by a different source than" properly reflects that the off-chip external clock and second clock "originate from a source other than" the ring oscillator clock and are accordingly "independent," as required by the '336 patent. This is entirely consistent with how TPL overcame Kato in reexamination. Kato disclosed CPU and I/O clocks that were generated by the same source, first clock (14). As Kato lacked independent clocks, it did not practice the '336 patent.

Plaintiffs do not explain how adding the confusing term "initially" before the word "generated" is helpful. Thesaurus.com sets forth that "generate" is a synonym for "originate." Just as a clock signal originates from one source, it is generated from one source. To permit for "initial generation" followed by "subsequent generation" – a corollary of Plaintiffs' construction – would offend the plain meaning of generate, and originate. Even the dictionary definition Plaintiffs cite does not include the word "initially." TPL's construction is correct.

F. "External Clock" (JCCS Row 24)

Plaintiffs have no rebuttal to TPL's specification support for its construction of "external clock," which adopts Judge Ward's definition. Plaintiffs selectively quote the prosecution history regarding Kato, while ignoring that the examiner "***agreed*** that adding the te[r]m 'off-chip' to ***clarify*** 'external'" would overcome prior rejections. '336 Reexam Hist., Mar Decl., Ex. G TPL0549462 (emph. added). TPL added the "off-chip" amendment "to further ***clarify*** the meaning of 'external clock,' noting its appreciation of the Examiners' "agreement" to the

clarification. *Id.* at TPL0549469 (emph. added).[11]

The undisputed specification evidence showing that "off-chip" and "external" mean the same thing (Op. Br. 29, n. 19), and the examiner's agreement that off-chip ***clarifies*** external, undercut Plaintiffs' attempt to construe this term so as to curtail damages under the doctrine of intervening rights. "An amendment that ***clarifies*** the text of the claim or makes it more definite without affecting its scope is generally viewed as identical." *Bloom Eng'g Co. v. N. Am. Mfg. Co.*, 129 F.3d 1247, 1250 (Fed. Cir. 1997) (emph. added); *see also Predicate Logic, Inc. v. Distributive Software, Inc.*, 544 F.3d 1298, 1305 (Fed. Cir. 2008) (citing *Bloom*). In this case, the "off-chip" amendments served only to clarify the "external" limitation of the original claims.

Plaintiffs' reliance on *Becton, Dickinson & Co. v. Tyco Healthcare Group, L.P.*, 616 F.3d 1249 (Fed. Cir. 2010) is misplaced. The general maxim of claim construction that all claim terms be given meaning is not inflexible. *Power Mosfet Techs., L.L.C. v. Siemens AG*, 378 F.3d 1396, 1409-10 (Fed. Cir. 2004) ("[W]here neither the plain meaning nor the patent itself commands a difference in scope between two terms, they may be construed identically."). As case law allows "clarifying amendments" in the context of intervening rights, it follows that all terms do not transform claim scope. The Court should adopt Defendants' construction.

G. The '749 Patent Does Not Require Operands To Be Right-Justified. (JCCS Rows 7, 12, 30)

1. Construction Of A Claim Term Not In The Patents-In-Suit, From A Patent Not In This Litigation, Is Irrelevant.

Plaintiffs' suggestion that Judge Ward's prior Markman Order requires the addition of the limitation that "operands" must be "right-justified in the instruction register"[12] does not disclose that the limitation comes from Judge Ward's construction of the coined term "instruction groups" not even in this litigation, from a separate invention, the '584 patent. In *ResQNet.com, Inc. v. Lansa, Inc.*, 346 F.3d 1374, 1382 (Fed. Cir. 2003), the Federal Circuit held that even where "related patents are similar, [but] their claims are not identical," courts must independently

[11] Plaintiffs also misinterpret TPL's arguments in overcoming Kato. TPL argued that the clock 15 in Kato was not an "external clock" because it was not "off chip." They did not argue that clock 15 was "not on the CPU," which would have been nonsense from a technical point of view.

[12] Plaintiffs insert this limitation into the claim terms "instruction register," "multiple sequential instructions," and "sequence of program instructions."

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

construe the claims in each patent. The '584 patent is a divisional patent of the '749 patent, meaning that the '584 patent carved out separate subject matter from its parent, the '749 patent. The '584 patent's "instruction groups" claim how instructions and data are organized in memory; the '749 patent claims how multiple sequential instructions are supplied to the CPU in a single memory cycle. Plaintiffs ignore the significant distinctions between the claims of the two patents, as they must, because it is the claims of a patent that defines the scope of the invention.

Independent claim 29's ***instruction groups*** contained an operand or instruction "located at a predetermined position from a boundary of [the] instruction groups."[13] Being able to locate the operand or instruction bits without addressing by having them at a predetermined location was critical for "certain" instructions groups to operate. Having operands in the instruction group be right-justified enabled the proper execution of certain instructions, *e.g.*, load short literal, or instructions that used variable-width-operands.

Claim 1 of the '749 patent, on the other hand, claims the "… means for fetching instructions … to fetch ***multiple sequential instructions*** from said memory in parallel and supply the ***multiple sequential instructions*** to said CPU integrated circuit during a single memory cycle …." '749 patent Cl. 1, Mar Dec., Ex. M. These claimed multiple sequential instructions are not the same as the '584 patent's instruction groups, as there is no limitation in Claim 1 requiring an operand to be located at a predetermined position as there was in Claim 29 of the '584 patent.[14]

Thus, Judge Ward's construction of "instruction groups," with its limitation on operands

[13] Although the '584 patent has since emerged from reexamination, Judge Ward construed original claim 29, which read: "[i]n a microprocessor system including a central processing unit, memory, and an instruction register, a method for providing instructions and operands from said memory to said [CPU] comprising the steps of providing ***instruction groups*** to said instruction register from said memory wherein certain of said ***instruction groups*** include at least one instruction that, when executed, causes an access to an operand or an instruction or both, said operand or instruction being located at a predetermined position from a boundary of said ***instruction groups***; decoding said at least one instruction to determine said predetermined position; locating said predetermined position; and supplying, from said instruction groups, using the predetermined location, said operand or instruction or both to said [CPU]." '584 patent, Cl. 29, Gupta Dec., Ex. 6.

[14] Plaintiffs' look to Judge Ward's claim construction of "instruction groups" from the '584 patent to construe "instruction register" in the '749 patent, ignoring that the parties in that case stipulated to a separate construction of "instruction register" that did not require operands to be right-justified: "[i]nstruction register means a hardware element that receives and holds an instruction group as it is extracted from memory; the register either contains or is connected to circuits that interpret the instructions in the group." Ward 8, Mar Dec., Ex. A.

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

in the context of a claim directed to "certain instructions," is inapplicable here.

2. The '749 Patent Discloses An Instruction That Encodes An Address That Is Not Right-Justified.

Plaintiffs dismiss TPL's example of an 8-bit instruction with a 4-bit opcode and a 4-bit operand that is not right-justified as not being an operand, because the word "operand" is not used, and because the Return Stack is not shown in Figure 4. These are red herrings.

a. An Address Within An Instruction Is An Operand.

"Operand" is not a claim term in this litigation (yet another reason why Plaintiffs' proposed construction is improper), but Judge Ward construed it as part of the '584 patent claims to be "an input to a single operation specified by an instruction that is encoded as part of the instruction where the size of the input can vary." Ward Order 24, Mar Dec., Ex. A. Judge Ward's construction for operand was essentially appropriate except that he included the limitation that "the size of the input can vary" to refer to the '584 patent's "variable width operands." The address bits of the example instructions TPL identified are "an input to a single operation specified by an instruction that is encoded as part of the instruction." They are thus operands. *See also, Dict. of Computer Terms* ("part of … instruction that contains the address … of data"), Gupta Dec., Ex. 7. To the extent Plaintiffs contend these operands must be right-justified, that construction reads out this embodiment, and such a construction is improper.[15] *See* cases at n.5.

b. Figure 4 Is Irrelevant.

Plaintiffs proffer no support for the proposition that the specification's disclosure of a non-right-justified operand is to be disregarded because it does not reference any structure shown in Figure 4 of the patent. Any such operand, encoded as part of an instruction and that is not variable-width, can be placed into the instruction register at any location. It is completely irrelevant that when these instructions execute, the CPU loads or stores items into the Return Stack. *See* '749 patent, 31:35-32:16, Mar Dec., Ex. M.

[15] Whether the xx and xxxx address bits of 8-bit instructions were operands was not at issue in the '584 patent litigation in Texas, and was, therefore not an issue on appeal to the Federal Circuit.

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

H. "Supplying Multiple Sequential Instructions In A Single Memory Cycle" (JCCS Row 5)

TPL and Plaintiffs both rely on the exact same passage in the prosecution history to support their proposed constructions. Plaintiffs, however, ignore the critical distinction by which TPL distinguished the Transputer references based on Edwards – supplying multiple instructions ***during a single memory cycle***. The patent owners argued that the Transputer only supplied instructions one-at-a-time from its prefetch buffer, and this could not meet the key limitation of delivering multiple instructions during a single memory cycle. '749 Reexam Hist., 26, Chen Dec. Ex. V. That limitation – during a single memory cycle – is already within the parties' agreed-upon claims construction. The only disclaimer is of a system that cannot supply multiple sequential instructions to a CPU during a single memory cycle.

Plaintiffs are wrong that TPL disclaimed "using a pre-fetch buffer or a one-instruction-wide instruction buffer that … supplies one instruction at a time." Opp. 25:25-27 (emph. added). As the quoted prosecution history shows, TPL disclaimed using a prefetch buffer and a one-instruction wide buffer. Most importantly, the parties all rely on the same passage for two different interpretations, thus showing the ambiguity, and supporting that there was no "clear and unequivocal" disavowal of a certain meaning. *Omega Eng'g Inc.*, 334 F.3d at 1324. The claim language requires only that multiple instructions be supplied during a single memory cycle, and that is precisely how TPL distinguished the Transputer references. Plaintiffs further ignore that the specification does not exclude systems containing a prefetch buffer. That the patent teaches being able to fetch and supply multiple instructions without using a prefetch buffer does not make it a claim limitation. *See*, cases at n.4.

I. "Exchanging Coupling Control Signals, Addresses And Data" (JCCS Row 18)

TPL's construction, by covering "transmitting and/or receiving …," correctly captures that coupling control signals, addresses and data are being transmitted, and/or received, or some combination thereof. Plaintiffs cannot dispute that Figure 6 depicts addresses flowing in only one direction in exchange for data in the other. Figures 3 and 11 of the patent also depict input/output exchanges wherein addresses are not received. Plaintiffs' construction reads out each of these

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

varieties of exchanging disclosed in the specification, which is improper.[16] *See* n.5. The dictionary definition of "exchange" that Plaintiffs themselves advance, "[t]o take or give in return for something ***else***," shows that an address can be taken in return for data and still be within the meaning of "exchanging." Chen Dec. Ex. Q (emph. added).

Plaintiffs' argument that "addresses and data … flow in ***both*** directions," is overly restrictive. Opp. 14:18-19. While Plaintiffs correctly note that buses 90 and 136 in Figure 17 allow for bidirectional exchange of addresses and data, neither the figure nor the specification indicates that addresses and data each flow bidirectionally. Even if they did, it would be improper to limit the claims to this embodiment. *See* cases at n.4.

J. "As A Function Of Parameter Variation" (JCCS Row 21)

TPL's claim construction is correct because the intrinsic evidence contemplates that clock rate/processing frequency can vary ***based on*** a variety of factors beyond those enumerated in the specification. The claim language states that processing frequency and clock rate vary in the same way "as a function of parameter variation in ***one or more*** fabrication or operational parameters…." '336 patent (Mar Dec., Ex. B), claim 6. This disjunctive phrase does not mandate that every parameter have an effect on clock rate or frequency. *See also*, claim 1 (emph. Added) ("varying…due to said manufacturing variations and due to ***at least*** operating voltage and temperature…"; claim 10 ("dependent upon variation in ***one or more*** fabrication or operational parameters …"). Nor must clock rate/frequency vary exclusively due to process technology, voltage and process, which are merely examples of parameters found in the specification.

Plaintiffs take an overly restrictive position by requiring that the parameter variation be "determined." Plaintiffs concede, however, that the specification describes no algebraic functions relating temperature, voltage, and process. In fact, there is a degree of randomness with microprocessors (even the support used by Plaintiffs states "the frequency will be in the

[16] *Boss Indus. v. Yamaha Motor Corp.*, 2:05-cv-422-DAK, 2007 U.S. Dist. LEXIS 98875, *12 (D. Utah Sept. 7, 2007) is distinguishable, because the court in that unpublished case refused to adopt a strained interpretation of a term in order to read in an embodiment. Here, Plaintiffs are proposing a strained construction of exchanging that contradicts their own proposed dictionary definition, and offering no reason at all why some embodiments of exchanging should be excluded.

neighborhood of …"). Indeed, over time permutations in the microscopic structure of the integrated circuit can cause performance changes. Furthermore, Plaintiffs do not dispute that their construction is confusing and contradicts the sense in which "functional relationship" was used in prosecution. For all of these reasons, TPL's proposal should be adopted.

K. "Operates Asynchronously To" (JCCS Row 29)

Plaintiffs disregard entirely that applicants introduced "asynchronously" during prosecution "to clarify the meaning of 'independent.'" '336 Reexam; Mar Decl., Ex. G at TPL0549470-71. Plaintiffs also overlook the required operational independence of the on-chip oscillator clocking the CPU and the second clock timing the I/O interface. Both the plain language of claim 11 and the specification describe "a second clock ***independent*** of the ring counter variable speed system clock." '336 patent, 3:27-28, 33-34; Mar Dec., Ex. B. TPL's construction captures how the two clocked circuits "operate asynchronously" of one another because their clock signals originate from different sources, are therefore independent clock signals, and thereby cause the clocked circuits to "operate asynchronously," as claimed.

There is no specification support for Plaintiffs' argument that "the CPU must operate without a timing relationship with the I/O interface" (Opp. 13:15), and indeed Plaintiffs cite none. That is because all clocks have a timing relationship to one another due to their periodic nature. For example, in a two-clock system, one clock will run x times faster than the other clock, thereby having a "timing relationship," whether intentional or not.

Plaintiffs improperly rely on an irrelevant statement made during prosecution regarding dependent claim 8, which required an external clock that "operates synchronously relative to said oscillator." Plaintiffs do not disclose that the applicants later canceled claim 8. Because the statement was made only with respect to a specific limitation in a now-canceled claim, it does not trigger any disclaimer with respect to the asserted claims. *Go-Light, Inc. v. Wal-Mart Stores, Inc.*, 355 F.3d 1327, 1332 (Fed. Cir. 2004). Defendants' construction should be adopted.

L. "Electronic Devices Correspondingly Constructed Of The Same Process Technology With Corresponding Manufacturing Variations" (JCCS Row 17)

Although Plaintiffs have proffered a new construction of this term in their Opposition

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

Brief, it is still wrong. Plaintiffs' new construction merely substitutes "with the same transistors on the same die under the same process parameters" for "the same process technology" in the claim language. This is an improper attempt to limit "process technology" to a particular description of an embodiment in the specification. As shown in the prosecution history, "process technology" was introduced to explain how the operating characteristics of electronic devices in a single integrated circuit will track one another depending on variations in the manufacturing process." Op. Br. 26:23-28. The key is not that the transistors are identical (or "the same"), it is that the transistors are manufactured together on the same silicon substrate, subject to the same manufacturing process technology, and therefore varying in the same way as a result of manufacturing variations. Defendants' construction should be adopted.

M. <u>"Means connected to said bus for fetching instructions" (JCCS Row 4)</u>

The parties agree that claim 1's multiple instruction fetch done in parallel is performed by the memory controller 118 and related circuitry. Op. Br. 23:22-24:11. Plaintiffs' proposal misapprehends the term "parallel" in claim 1, conflating it with the "fetch-ahead" aspect of the '749 invention, which is found in claim 2, and incorrectly includes claim 2's fetch-ahead circuitry 192, 194, 196 within claim 1.[17] *See* '749 patent, 7:50-8:16, Mar Dec., Ex. M. Because it includes the structure corresponding to claim 2 in claim 1, Plaintiffs' construction is wrong. *Phillips*, 415 F.3d at 1324-25 (claim construction rendering dependent claim "redundant" wrong).[18]

Dependent claim 2 "***additionally compris[es] means*** connected to [claim 1's] means for fetching multiple instructions ***for determining by decoding … if multiple instructions fetched by [claim 1's] means … require a memory access, [claim 1's means performing a fetch] if decoding … shows that the multiple instructions do not require a memory access.***" '749 patent,

[17] The file history confirms fetch-ahead is distinct from parallel fetch. *See* '749 patent, 22:11-40, Mar Dec., Ex. M; '749 Pros. Hist., Gupta Dec., Ex. 3, TPL0001064 (distinguishing and contrasting "overlapping instruction fetch and execution" in prior art and "fetching multiple sequential instructions in parallel during a single memory cycle…" of Moore invention).

[18] Confirming that "parallel fetch" refers to the multiple sequential instruction fetch is that the bus width is claimed as being at least equal to the number of bits in each of the instructions times the number of instructions ***fetched in parallel in a single memory cycle***. In microprocessor 50, this corresponds to the 8-bits in each instruction time the four instructions fetched in parallel, mandating at least a 32 bit bus. *See* '749 patent, 7:12-15, Mar Dec., Ex. M ("The microprocessor 50 fetches 4 instructions per memory cycle; the instructions are in an 8-bit format, and this is a 32-bit microprocessor. System speed is therefore 4 times the memory bus bandwidth.").

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

Claim 2 (emph. added).

The corresponding structure to this "fetch-ahead" functionality is "decoder 192 [] connected to memory controller 118 by line 196." *Id.*, 7:65-66. The specification provides that, "The output of decoder 192 on line 196 requests an instruction fetch ahead by memory controller 118" when "there are no memory reference instructions in the queue." *Id.*, 8:4-8. If, as Plaintiffs propose, claim 1 included the decoding means of 192, 194 and 196, its scope would be the same as dependent claim 2, contrary to the teaching of *Phillips*.

As parallel fetch can operate without fetch-ahead, 192, 194 and 196 are not essential to claim 1, and are not part of the corresponding structure for claim 1. *Micro Chem., Inc. v. Great Plains Chem. Co.*, 194 F.3d 1250, 1258 (Fed. Cir. 1999) (Section 112, ¶ 6 does not "permit incorporation of structure from the written description beyond that necessary to perform the claimed function."); *see Versa Corp. v. Ag-Bag Int'l Ltd.*, 392 F.3d 1325 (Fed. Cir. 2004) (applying claim differentiation to find that structure corresponding to dependent claim 2 is not necessary for claim 1, because if it were, claim 2 would be redundant); *Asyst Technologies, Inc. v. Empak, Inc.*, 268 F.3d 1364, 1372 (Fed. Cir. 2001), is inapposite because the connecting lines in that case were essential to performance of the functions being construed.

N. "Multiplexing means …" (JCCS Row 6)

Plaintiffs conclusorily assert that TPL's proposed construction of the function is unsupported. They fail however, to address Figure 11 of the specification, which clearly shows that different types of information can be placed onto the bus at different times. They also ignore the prosecution history cited by TPL. *See* '749 Reexam Hist.; Mar Dec. Ex. Q, TPL0554297-298. A23-A13 and A12-A2 are nowhere mentioned in the passage of the specification discussing the multiplexer, and are accordingly non-essential. '749 patent, 14:66-15:21, Mar Dec., Ex. M. *Micro Chem,* 194 F.3d at 1258. In *Asyst* the connecting line was not only in the figure, but also discussed in the written description, which made that structure distinguishable.

III. CONCLUSION

Defendants request the Court adopt TPL's proposed claims constructions.

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400

Dated: February 11, 2011

FARELLA BRAUN & MARTEL LLP

I represent that concurrence in the filing of this document has been obtained from each of the other signatories which shall serve in lieu of their signatures on this document.

By: /s/
John L. Cooper

Attorneys for Defendants
TECHNOLOGY PROPERTIES LIMITED and ALLIACENSE LIMITED

Dated: February 11, 2011

KIRBY NOONAN LANCE & HOGE LLP

By: /s/
Charles T. Hoge, Esq.

Attorneys for Defendant
PATRIOT SCIENTIFIC CORP.

Farella Braun + Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954-4400